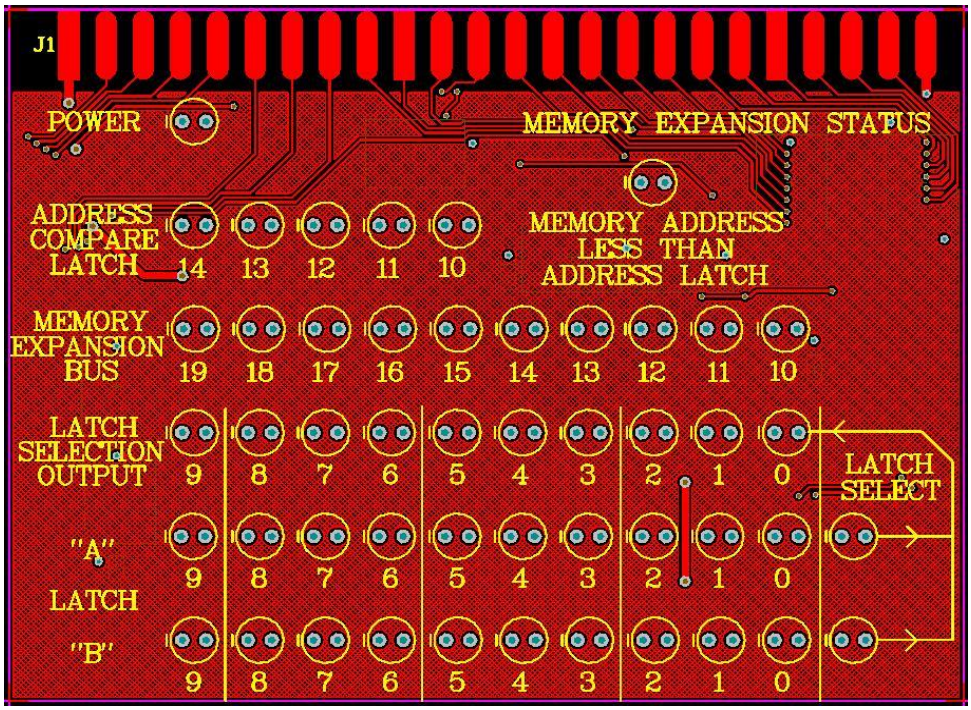
Simple Dynamic Mapping System

Because there is very little information in the 5420 and 5423 manuals about the dynamic mapping system which manages the memory bank switching system the purpose of this document gain some understanding of the operation of the DMS.



Above is the Memory Expansion Status board I made and this will allow me to monitor the Simple DMS status as I execute code to test the DMS operation.

Starting the assessment of the DMS status board, assuming all is working correctly. From power on reset the following status was displayed:

> Address comparison latch bits 10-14 are all 1's.
> Address latch A bits 0-9 are all 0's
> Address latch B bits 0-9 are all 1's
> Output latch bits 0-9 are all 1's
> Latch 'B' is selected.
> Memory Address less than Address Latch (OFF)
> Memory Expansion Bus bits 11-14 are 1's, while bits 19-15 and 10 are 0's, bit 10 appears to operate on startup when the micro-code appears to be performing a memory test.

Now having read the HP description for the Dynamic Mapping System Board (DMSB) 05443-60057 and found part of the description to be wrong I've gone back to one of my source documents "HP 12731A MEMORY EXPANSION MODULE", "Theory of Operation". On page V-30 the relevant signals are described:

MEST- Memory Expansion Store, low true
Origin: CPU
Timing: MEST- is generated whenever MEU is in the store field of any microinstruction.

MESP- Memory Expansion Special, low true
Origin: CPU
Timing: MESP- is generated whenever MESP micro-order is in the special field of any microinstruction.

The following is a detailed disassembly of the two simplified DMS instructions.

Instruction 105573 @ address 5460 in micro-code module 11

```
5460    PASS S9 P                   ; save the program counter

        P   places (P) onto S-Bus
        S9      Stores data on S-Bus to S9 (scratch pad)
        PASS    Passes data on S-Bus to ALU without modification

5461    READ INC PNM A              ; (A) points to memory loc with Latch "A" data.

        A  places (A) onto S-Bus
        PNM     Store data on S-Bus to M reg, INC S-Bus, Store T-Bus to P reg
        INC     Specifies the INC instruction for the ALU
        READ    Read the contents of Memory pointed to by M reg

5462    MESP PASS  TAB              ; Set Latch "A"

        TAB     Places the result of the read on S-Bus
        PASS    Passes data on S-Bus to ALU without modification
        MESP    MESP (only) triggers latch "A"

5463    READ PASS M P               ; (P) points to memory loc with Latch "C" data.

        P   places (P) onto S-Bus
        M Store data on S-Bus to M reg
        PASS    Passes data on S-Bus to ALU without modification
        READ    Read the contents of Memory pointed to by M reg

5464    PASS MEU TAB                ; Set Latch "C"

        TAB     Places the result of the read on S-Bus
        MEU     MEU (only) triggers latch "C"
        PASS    Passes data on S-Bus to ALU without modification

5465    RTN PASS P S9               ; Restore the program counter and return

        S9      places (S9) onto S-Bus
        P   Stores data on S-Bus to P reg
        PASS    Passes data on S-Bus to ALU without modification
        RTN     Returns from subroutine
```

Instruction 105574 @ address 5373 in micro-code module 10, called from micro-code module 11

```
5373    PASS S9 P                   ; save the program counter
```

P places (P) onto S-Bus
S9 Stores data on S-Bus to S9 (scratch pad)
PASS Passes data on S-Bus to ALU without modification

5374 READ INC PNM A ; (A) points to memory loc with Latch "B" data.

A places (A) onto S-Bus
PNM Store data on S-Bus to M reg
INC S-Bus, Store to P reg
READ Read the contents of Memory pointed to by M reg

5375 MESP PASS MEU TAB ; Set Latch “B”

TAB Places the result of the read on S-Bus
MEU MEU
PASS Passes data on S-Bus to ALU without modification
MESP MESP with MEU ; triggers Latch “B”

5376 S9 P PASS RTN

S9 places (S9) onto S-Bus
P Stores data on S-Bus to P reg
PASS Passes data on S-Bus to ALU without modification
RTN Returns from subroutine

The next table lines up the micro-instruction step numbers with the hardware signals, note where OP, SPECIAL, ALU, STORE, and S-BUS parts of the microcode are left blank this means “don’t care”.

OP	SPECIAL	ALU	STORE	S-BUS	MESP-	MEST-	MICRO-INSTR
	MESP		MEU		0	0	5375
	MESP				0	1	5462
			MEU		1	0	5464

The next table lines up the MEST* and MESP* signals with the latches that are clocked.

MEST-	MESP-	LATCH	Microcode Lines
0	0	“B”	5375
1	0	“A”	5462
0	1	“C”	5464

Now the lines of micro-instruction code in the last table are executed by the following macrocode opcodes

Opcode 105573 executes line 5462 then 5464.

Opcode 105574 executes line 5375.

The other lines of code referenced by the two macrocode opcodes are support functions like preparing data to be latched, saving the program counter, returning from subroutine, etc. The above lines actually clock the latches on the DMS PCB.

In the code fragment below the operation of latching data into the three latches is shown, prior to executing 105573 A-reg contains a pointer to the first of two data words, the data in A.REGISTER is latched into Latch A when line 5462 of microcode is executed and the pointer is incremented to point to C.REGISTER and the data in C.REGISTER is latched into Latch C when line 5464 of microcode is executed. Next, prior to executing 105574 A-reg contains a pointer to the data in B.REGISTER is latched into Latch B when line 5375 of microcode is executed.

```
*
*-------------------------------------------------------------------------------------------------
*
*       SET SIMPLIFIED DMS HARDWARE USED IN THE
*       HP 5420A AND 5423A DIGITAL SIGNAL ANALYZERS
*
*-------------------------------------------------------------------------------------------------
*
SET.SDMS    NOP
            LDA   A.POINTER   ; Point to A & C mapping register data
            SAL               ; Opcode 105573 (SAL is my mnemonic)
            LDA   B.POINTER   ; Point to B mapping register data
            SBL               ; Opcode 105574 (SBL is my mnemonic)
            JMP   SET.SDMS,I
A.POINTER   DEF   *+1         ; This defines the address of the memory location
                              ; of the A.REGISTER (A Latch Register) and the
                              ; next contiguous memory location must contain
                              ; the data for C.REGISTER comparison register
A.REGISTER  OCT   0           ; A Latch data
C.REGISTER  OCT   20          ; C Latch data
                              ; Both A & C latch data must be present before
                              ; the SAL instruction is executed.
B.POINTER   DEF   *+1         ; This defines the address of the memory location
                              ; of the B.REGISTER  (B Latch Register)
B.REGISTER  OCT   0           ; B Latch data
*
```

The hardware on the DMS board calculates the extended memory address from A latch if M-Bus bits 14-10 are less than Latch C data, and B latch is used to calculate the extended memory address M-Bus >= to Latch C.

Now added the HP explanation about the DMS board:

The “A0” Register (Latch A) holds the starting address of one segment of memory.
The “AL” Register (Latch C) holds the length of that segment.
The “B0-AL” Register (Latch B) holds the starting address of the second segment minus the length of the first segment. The subtraction is necessary because the new address is the sum of the “basic” address plus either the first segment register of the second. When the “basic” address is equal to or greater than the length “AL”. The new address is “(B0-AL)+M”. At the point where M=AL, the new address is “B0”.

The new address is called the “MEB” (“Memory Expansion Bus”), and is 20 bits wide. The ten most-significant bits are constructed by the board. The ten least-significant bits come from the ten least-significant bits of the 5443A's M-Bus.

A PRESET on the 5443A clears all three registers to zero.

From a programming perspective all of the numbers used when setting the DMS should be in units of 2k word page boundaries (1024 base 10).

So A0, Latch A contains segment one, page start.
AL, Latch C contains the segment length in the number of pages.
B0-AL, Latch B, contains segment two, page start minus the segment length (AL).